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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,853	07/31/2003	Han-Jong Kim	2557-000168/US	1965

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EXAMINER	
ABBASZADEH, JAWEED A	

ART UNIT	PAPER NUMBER
2115	

MAIL DATE	DELIVERY MODE
06/27/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/630,853	KIM, HAN-JONG	
	Examiner	Art Unit	
	JAWEED A. ABBASZADEH	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-21 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-5 and 7-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The rejection as set forth in the previous office action is hereby maintained and incorporated by reference.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Tomiyori US 5,475,324.

As to claim 1, Tomiyori teaches a processor having a processor core and at least one peripheral device [a clock can be provided an arbitrary number of different devices], comprising:

a selecting circuit [Fig. 1, 30, 60] for determining at least one of operation states and operating frequencies of a high-speed control circuit [Fig. 1, 10, 11, 40] and a low-speed and low-power control circuit [Fig. 1, 20, 21, 40] based on direct monitoring of the high-speed control circuit and the low-speed and low-power control circuit and for outputting a selection signal based on the determination [col. 2, lines 62-68—col. 3, lines 1-8];

the high-speed control circuit for controlling high-speed operations of at least one of the processor core and the peripheral device in response to the selection signal; and

the low-speed and low-power control circuit for controlling low-speed and low-power operations of at least one of the processor core and the peripheral device in response to the selection signal [col. 3, lines 62-67—col. 4, lines 1-3].

As to claim 2, Tomiyori teaches the high-speed control circuit controls the high-speed operations of one of at least the processor core and the peripheral device if the determination indicates the processor is operating in a normal mode, and the low-speed and low-power control circuit control the low-speed and low-power operations of one of at least the processor core and the peripheral device if the determination indicates the processor is operating in a slow mode [col. 3, lines 62-67—col. 4, lines 1-3].

As to claim 3, Tomiyori teaches the selecting circuit compares an operating frequency of the processor with a predetermined threshold frequency to obtain a compared result and outputs the selection signal based on the compared result [col. 4, lines 61-67].

As to claim 4, Tomiyori teaches the high-speed control circuit controls the high-speed operations of one of at least the processor core and the peripheral device when the operating frequency of the processor is higher than the predetermined threshold frequency, and the low-speed and low-power control circuit controls the low-speed and low-power operations of one of at least the processor core and the peripheral device when the operating frequency of the processor is lower than the predetermined threshold frequency [col. 4, lines 61-67].

As to claim 5, Tomiyori teaches the processor core is a central processing unit (CPU) [It is well known in the art to consider a processor core as being a central processing unit].

As to claim 6, Tomiyori teaches the peripheral device is at least one of a wireless LAN card, a PC card, and a liquid crystal display (LCD) [These are well known peripheral devices].

As to claim 7, Tomiyori teaches this claim according to the reasoning set forth in claim 1. Furthermore, using a multiplexer as an interface falls under design choice. Tomiyori uses a switch as an interface while the present invention uses a multiplexer to act as a switch.

As to claims 8-9, Tomiyori teaches these claims according to the reasoning set forth in claims 2 and 4.

As to claim 10-12, Tomiyori teaches these claims according to the reasoning set forth in claims 1, 3-5, and 7.

As to claim 20, Tomiyori teaches the apparatus as set forth in claim 1. As such, Tomiyori teaches the method to operate the apparatus.

As to claim 21, Tomiyori teaches the high-speed control circuit is in an active state before the selecting circuit makes the determination if the determination indicates to output the selection signal to select the high-speed control circuit [col. 2, lines 31-40]. The high-speed control circuit is active in this case before switching because the clock switching control means waits until **the clock becomes stable** before switching can occur.

Response to Arguments

Examiner respectfully maintains the rejection in regards to 35 USC 112 first paragraph. The term "processor" as defined in the specification goes beyond a reasonably accepted meaning. Specifically, using the term "processor" to contain such peripheral devices including a wireless LAN card and liquid crystal display. Although Applicant may choose to call element 200 whatever Applicant chooses, the designation of a processor must fit within a reasonable accepted meaning in the art.

Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAWEED A. ABBASZADEH whose telephone number is

(571)270-1640. The examiner can normally be reached on Mon-Fri: 7:30 a.m.-5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jaweed A Abbaszadeh/
Examiner, Art Unit 2115
6/19/2008

/Thomas Lee/
Supervisory Patent Examiner, Art Unit 2115